Press Release

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Eureka Delivers IP Cores for Cypress's Delta39K™ CPLDs

SDRAM Controller and PCI Cores Target High-Speed Communications System Designs

SAN JOSE, California…April 4, 2001 – Cypress Semiconductor (NYSE: CY) and Eureka Technology today announced that Eureka has delivered to the Cypress IP Oasis program two intellectual property (IP) cores for the Cypress Delta39K™ family of complex programmable logic devices (CPLDs). Optimized Eureka netlists for Cypress Delta39K programmable devices will simplify the CPLD's integration into system designs, dramatically accelerating time-to-market for applications in the high-growth data communications, telecommunications, computation, and consumer markets.

The EP520 SDRAM controller core and EC125 32-bit PCI Target core, both available in netlist and RTL source code formats, are the first cores delivered under a partnership agreement announced in the last quarter of 2000. The cores are optimized for use in Cypress's HDL-based *Warp*™ design tool, which integrates graphical capturesimulation, synthesis, ,andmanagement .

"Cypress's Delta39K is the first true high-density CPLD family to offer IP, and the Eureka cores support our strategy to provide our customers with a complete solution," said Geoff Charubin, Cypress director of marketing. "Our customers in the communications arena usually have small windows of opportunity to deliver systems, and robust support for the Delta39K and its unique architecture minimizes design complexity and shortens time-to-market."

"These cores are the first in a series that Eureka will bring to Cypress's IP Oasis program, reinforcing our strategy to support programmable devices with silicon-proven and production-proven IP cores," said Simon Lau, president of Eureka Technology. "As Eureka continues to add to the growing

library of pre-qualified offerings for the Delta39K devices, designers can shift their focus from tactical, gate-level issues to broader design issues."

The Cores

The EP520 SDRAM controller core is a fully-programmable, zero-wait-state, SDRAM control interface that supports multiple external memory banks for standard SDRAM devices (PC100/133 SDRAM DIMM and discrete SDRAM chips) ranging in density from 16 to 256 Mbits. The controller core supports programmable access timing parameters, programmable burst length and automatic refresh generation with user-defined refresh intervals.

The EC125 PCI Target core is a flexible, highly efficient, 32-bit PCI interface to back-end user applications. It supports PCI-specification 2.1 and 2.2 protocols. Its flexible back-end bus simplifies integration with user logic. The additional flexibility provided by zero-wait-state and user-inserted wait-state burst-data transfers help maximize memory bandwidth. The core uses a double data buffer design approach that minimizes design gate count while achieving the highest possible data bandwidth.

IP Oasis

The IP Oasis program was designed to be the primary portal for data communications solutions built with IP/Cores and Cypress programmable logic devices, such as the Delta39K family of CPLDs and the PSI™ family of programmable PHYs. The IP/Cores are targeted at a variety of applications, including backplanes, linecards, switches, routers, 3G basestations, VoIP gateways, servers, mass storage equipment, interconnecting workstations, and video-transmission equipment. The cores are available as netlists optimized for use with Cypress's *Warp* development environment. IP Oasis, located at http://www.cypress.com/pld/ipoasis, allows users to view and select prequalified intellectual property cores and directs visitors to the IP vendor's sites for licenses and downloads.

Cypress Delta39K Family of CPLDs

Cypress's Delta39K CPLDs offer up to 350,000 usable gates, approximately ten times the size of today's largest CPLD. The family offers more embedded memory – 240 Kbits for the 100,000-gate Delta39K100 and 480 Kbits for the 200,000-gate Delta39K200 – than any other programmable logic device, including even the largest field-programmable gate arrays (FPGAs). Delta39K is also the first programmable logic device to embed First-In First-Out (FIFO) control and dual-port memory arbitration logic into each specialty memory block. This significantly reduces the logic required, increases the system performance, and speeds the design cycle of any application utilizing FIFO or dual-port memory.

Licensing and Availability

The SDRAM controller and PCI Target cores for Cypress's line of high-performance CPLDs are available for licensing directly through Eureka Technology's Web site, located at http://ww.eurekatech.com/partners/cypress.htm.

The PowerPC Suite of cores is scheduled to be introduced later this year, including a PCI host bridge, PowerPC bus master, PowerPC bus slave, and PowerPC bus arbiter. For more information on the Eureka core portfolio, please call (650)960-3800 or visit the Eureka Technology Web site (http://www.eurekatech.com)or Cypress's IP Oasis Web site (http://www.cypress.com/pld/ipoasis). For more information on Cypress CPLDs, customers can call (800)858-1810 in the U.S. or (408)943-2600, or visit http://www.cypress.com.

About Cypress

Cypress Semiconductor (NYSE: CY) is "Driving the Communications Revolution"™ by providing high-performance integrated circuit solutions to fast-growing markets, including data communications, telecommunications, computation, consumer products, and industrial control. With a focus on emerging communications applications, Cypress's product portfolios include networking-optimized and micropower static RAMs; high-bandwidth multi-port and FIFO memories; high-density programmable logic devices; timing technology for PCs and other digital systems; and controllers for Universal Serial Bus (USB). More information about Cypress is accessible electronically on the company's worldwide Web site at http://www.cypress.com or by CD-ROM (call 1-800-858-1810).

"Safe Harbor" Statement under the Private Securities Litigation Reform Act of 1995: Statements herein that are not historical facts are "forward-looking statements" involving risks and uncertainties, including by not limited to: the effect of global economic conditions, shifts in supply and demand, market acceptance, the impact of competitive products and pricing, product development, commercialization and technological difficulties, and capacity and supply constraints. Please refer to Cypress's Securities and Exchange Commission filings for a discussion of such risks.

About Eureka Technology

Eureka Technology is a leading intellectual property (IP) provider for PLD and ASIC designers. The company offers a wide range of silicon-proved system core logic functions and peripheral functions for systems based on PCI bus, PowerPC, ARM, MIPS, ARC, or SH2-4 CPUs. These IP cores are designed to improve the design time-to-market delay, eliminate design risks, and reduce development costs. Founded in 1993, the company has a strong customer base in the United States, Japan and Europe. For more information about the company, please visit the Web site at http://www.eurekatech.com or send email to info@eurekatech.com.

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